Biased Voting for Improved Yield in Nanoscale Fabrics

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***Abstract*—Various fault-tolerance techniques have been proposed in recent years to tolerate the high defect rates expected in emerging nanofabrics with unconventional nano-manufacturing techniques. The proposed techniques include modular redundancy schemes that use majority voters to vote on the '0' or 1' outputs of redundant modules. Novel nanoscale computational fabrics employ new circuit and logic styles where the likelihood of occurrence of faulty '1's and faulty '0's may not be identical. This provides an opportunity for using biased voting (towards logic '1' or '0') to achieve improved yield. In this paper, we investigate the effectiveness of using biased voters as opposed to majority voters in such nanoscale fabrics. We analyze the Nanoscale Application Specific Integrated Circuits (NASIC) fabric and show that faulty '1's may be up to 12x more likely than faulty '0's, paving the way for applying biased voting successfully. For NASIC modules with a fan-in of 10, biased voting configurations are shown to achieve more than 27% increase in the probability of producing a correct output.**

Keywords: Biased Voting, TMR, NASICs, Fault Probability Ratio, Yield, Signal Reliability

I. INTRODUCTION

A variety of nano-materials and nano-devices including semiconductor nanowires [1],[2], carbon nanotubes [3], quantum cellular automata (QCA) [4], graphene-based devices [5], spin-wave fabrics [6] and molecular devices [7] have been proposed as alternatives to conventional CMOS. However, self-assembly and unconventional manufacturing approaches for scalable assembly of nanostructures may imply orders of magnitude higher defect rates compared to CMOS [8]. Therefore, built-in fault tolerance techniques need to be incorporated in nanoscale systems at various levels to achieve high-yield systems. Different fault tolerance approaches have been proposed in the past, such as error-correcting codes, n-way structural redundancy [9],[11], triple modular redundancy (TMR) and N-tuple modular redundancy (NMR) [17]. Fault tolerance techniques combining modular and structural redundancy have also been proposed and evaluated [18].

In modular redundancy techniques, identical replicas of modules are created whose outputs are then voted upon. For instance, in TMR, the outputs of three identical copies of a (non-redundant) module are fed into a majority voter. If, for example, at least two of the three modules produce logic '0's, then the voter outputs a '0'. Otherwise, the voter outputs logic '1'. The inherent assumption that is made, when majority voters are employed, is that a '0' to '1' fault (referred to as faulty '1' henceforth for convenience) is as likely as a '1' to '0' fault (faulty '0'). In other words, it is assumed that defects within the computational fabric may cause faulty '0's and faulty '1's with equal probability. However, with nanoscale computation fabrics based on novel circuit and logic styles, and different defect scenarios due to unconventional manufacturing, this assumption may no longer be valid. One type of faults may be more frequent than another. This provides an opportunity to potentially achieve higher yields by using biased voters, i.e., by offering greater protection against the most likely faults and less against the others. For instance, if faulty '1's are more likely than faulty '0's, the voting decision may be biased towards fewer logic '0' signals from input modules, thereby tolerating more faulty '1's.

In this paper we compare biased voters to traditional majority voting in such cases where the probabilities of faulty '0's and faulty '1's are unequal. We show that as the imbalance between the two fault probabilities is increased, the biased voting schemes become more effective. To illustrate these schemes, we study the fault mechanisms in the NASIC [9]-[12] nanoscale fabric, and show that such an imbalance between fault types does indeed exist. We then demonstrate that by using biased voting configurations we can increase the probability of producing a correct system output. While the evaluation was carried out for NASICs, biased voting schemes are generically applicable to other computing fabrics where imbalance between rates of faulty '1's and '0's exists.

The rest of the paper is organized as follows. Section 2 presents comparison of biased voting schemes to majority voting schemes when one type of faults becomes more likely than the others. Section 3 takes NASICs as an example fabric and shows that faulty '1's are more likely than faulty '0's. Section 4 shows the results of applying biased voters to the NASIC fabric and Section 5 concludes the paper.

II. BIASED VOTING – GENERAL CASE

Figure 1 shows a TMR and a biased voting configuration. The key difference between the two is the voting decision: in the first case (TMR) a majority voter is used to vote on three structurally non- redundant input modules whereas in the second, a

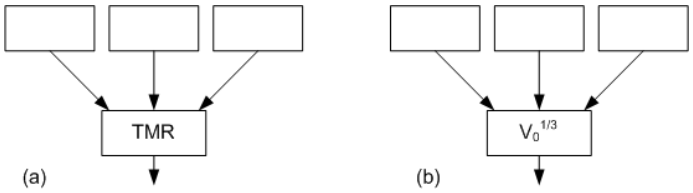


Figure 1. Voting configurations: (a) TMR majority voting, (b) $V_0^{1/3}$ biased voting

voter biased towards a single logic '0' is used. The notation used for this biased voter is $V_0^{1/3}$ (voter biased towards logic '0' that will produce logic '0' even if only 1 out of the 3 inputs is '0'). A biased voter has a lower (higher) tolerance for the less (more) prevalent fault type. For instance, the $V_0^{1/3}$ biased voter will not be able to tolerate any faulty '0's but can tolerate up to two faulty '1's.

Our objective is to find out whether the use of a biased voter instead of a conventional majority voter can enhance the expected yield of the voting configuration. Yield is the probability that the circuit will produce a correct output in the presence of manufacturing defects. The two voting configurations (shown in Figure 1) use the same three non-redundant nano-modules. Thus, the difference in the probability of producing a correct output by the two circuits will be due to the different voting schemes. Such an accurate comparison between the two voting schemes and their corresponding voter designs can be achieved by using the Signal Reliability metric [15],[16].

In the following analysis, faults in voters are not considered. Their affect on majority and biased voting schemes are expected to be substantially the same and have been omitted in this study to simplify the resulting expressions. This is because the biased voter and its majority voter counterpart have roughly the same fan-in and complexity. For example, the TMR and $V_0^{1/3}$ both have a fan-in of 3. Furthermore, a number of techniques have been proposed to increase the reliability of voting schemes in general. These include multiplying the voter three times and connecting the module outputs to all three voters [17],[19] and incorporating on-line self-testing into voters [20],[21]. All such techniques are equally applicable to both majority and biased voters.

To derive the probabilities of producing correct '0' and '1' outputs by the two voting configurations we use the following notations:

- V^C Correct output from the voter if it were to take inputs from defect-free input modules
- V^A Actual output from the voter taking inputs from defective input modules
- $P_{i/j}$ Conditional probability of getting a module output of i given that the correct module output should have been j ($i,j=0,1$). Clearly, $P_{0/j}+P_{1/j}=1$, for $j=0,1$.
- SR Signal Reliability: Probability of a correct output from a voter taking inputs from defective modules

A correct '0' ('1') will be produced by a TMR if all three inputs to the voter (from the modules) are correct '0's ('1's) or if any two of the inputs are correct '0's ('1's). The probabilities that a TMR generates correct '0's and '1's are

$$P(V^A=0|V^C=0)_{TMR} = (1-P_{1/0})^3 + 3P_{1/0}(1-P_{1/0})^2 = (P_{0/0})^3 + 3P_{1/0}(P_{0/0})^2 \quad (1)$$

$$P(V^A=1|V^C=1)_{TMR} = (1-P_{0/1})^3 + 3P_{0/1}(1-P_{0/1})^2 = (P_{1/1})^3 + 3P_{0/1}(P_{1/1})^2 \quad (2)$$

Similarly, probability expressions for the $V_0^{1/3}$ biased voter can be derived,

$$P(V^A=0|V^C=0)_{V01/3} = (1-P_{1/0})^3 + 3P_{1/0}(1-P_{1/0})^2 + 3P_{1/0}{}^2(1-P_{1/0}) = (P_{0/0})^3 + 3P_{1/0}(P_{0/0})^2 + 3P_{1/0}{}^2P_{0/0} \quad (3)$$

$$P(V^A=1|V^C=1)_{V01/3} = (1-P_{0/1})^3 = P_{1/1}{}^3 \quad (4)$$

Note that the conditional probabilities, $P_{1/0}$ and $P_{0/1}$, are due to defects occurring in the modules and not in the voters. Their values are dependent on the defect rate, defect model and the circuit and logic styles of the nano-fabric considered.

The signal reliability of the voter's output can be expressed as:

$$SR = [P(V^A=0|V^C=0)]\,P(V^C=0) + [P(V^A=1|V^C=1)]\,P(V^C=1) \quad (5)$$

The signal reliability expressions for the TMR and $V_0^{1/3}$ can be obtained by substituting (1), (2), (3), (4) into (5). In a similar manner, the signal reliability for other majority and biased voting configurations can be found. It is evident from (5) that the signal reliability not only depends on the probability of faulty '1's and '0's produced by the input modules but also on

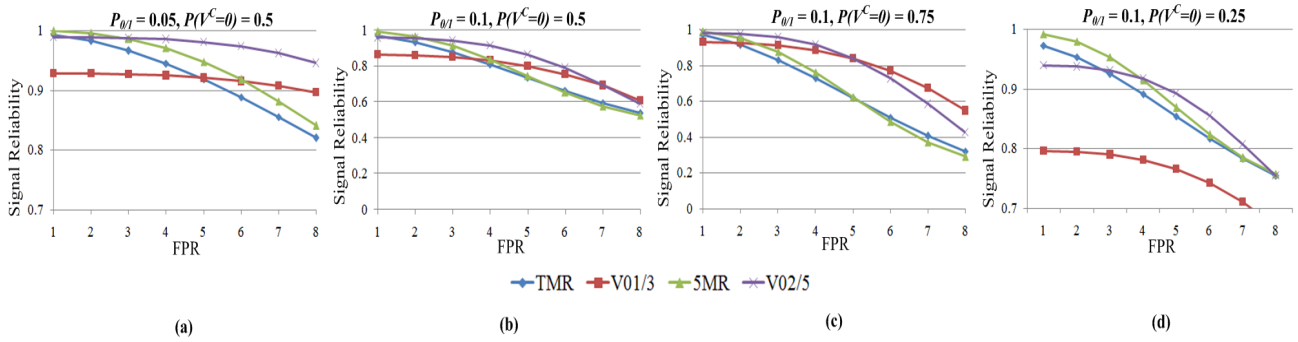


Figure 2. Signal reliability as a function of Fault Probability Ratio (FPR) for (a) $P_{0/1} = 0.05$, $P(V^C=0) = 0.5$ and (b) $P_{0/1} = 0.1$, $P(V^C=0) = 0.5$ (c) $P_{0/1} = 0.1$, $P(V^C=0) = 0.75$ and (d) $P_{0/1} = 0.1$, $P(V^C=0) = 0.25$

the number of input patterns that should correctly generate '0's and those that should correctly generate '1's. Figure 2 shows the signal reliabilities for four different voting schemes over a range of Fault Probability Ratios (*FPR*), where the FPR is the ratio between the probability of a faulty '1' to the probability of a faulty '0', i.e., FPR = $P_{1/0}/P_{0/1}$. The $V_0^{2/5}$ biased voting scheme is biased towards 2 '0's out of the 5 inputs and the 5MR is a majority voting scheme voting on 5 redundant inputs. Figures 2(a) and 2(b) show the signal reliability for $P_{0/1}$ values of 0.05 and 0.1, for a symmetric function where $P(V^C=0)=P(V^C=1)=0.5$. However, it is also possible for a logic functions to be skewed towards '1' or '0' in terms of correct outputs. Figures 2(c) and 2(d) show the signal reliabilities for the cases where $P(V^C=0)=0.75$ and $P(V^C=0)=0.25$, respectively.

As can be seen from Figures 2(a) and 2(b), the biased voting schemes ($V_0^{1/3}$ and $V_0^{2/5}$) have a higher signal reliability compared to their corresponding majority voting schemes (TMR and 5MR, respectively) with increasing *FPR*. As the probability of a faulty '1' rises compared to that of a faulty '0', the voters biased to logic '0' will be more likely to produce a correct output. For example, in Figure 2(b) where $P_{0/1} = 0.1$ with $P(V^C=0)=P(V^C=1)=0.5$, the $V_0^{2/5}$ scheme has 20% higher signal reliability than the 5MR majority scheme while the $V_0^{1/3}$ biased scheme has a 16% higher signal reliability than the TMR at FPR=7.

The $V_0^{2/5}$ scheme exhibits higher signal reliability than 5MR for FPR $\geq$ 3, whereas for the $V_0^{1/3}$ scheme the benefits over TMR are achieved only for FPR > 4. This is due to the comparatively poor resilience of the latter scheme to faulty '0's, since a single faulty '0' causes diminished reliability in that scheme. In this case, the probability of generating correct '1's at the output of the voter is the dominating factor. On the other hand, for FPR > 7, the faulty '1' probability is much higher and the requirement for 2-out-of-5 '0's for the $V_0^{2/5}$ voter is harder to achieve. However in the case of the $V_0^{1/3}$ voter, a single correct '0' is sufficient to ensure a correct final output implying that the overall reliability is higher. The probability of generating correct '0's is the dominating factor in this scenario.

In situations where $P(V^C=0) \geq P(V^C=1)$ such as the case shown in Figure 2(c), the frequency of occurrence of faulty '1's (0's) is further increased (reduced). At an FPR of 7, a 57% increase in reliability is attained by the $V_0^{2/5}$ scheme over the 5MR while a 66% increase in reliability is demonstrated by the $V_0^{1/3}$ scheme over the TMR. Figure 2(d) shows the opposite case where $P(V^C=1) \geq P(V^C=0)$. Here the frequency of occurrence of faulty '1's is reduced while that of faulty '0's is increased. The $V_0^{2/5}$ scheme is still able to show a higher reliability from an FPR value of 4 up to 8. On the other hand, the $V_0^{1/3}$ scheme shows low reliability because of its inability to tolerate even a single faulty '0'. This suggests that a higher reliability maybe attained by switching the bias of the voters from logic '0' to '1'. However, in nanoscale fabrics that implement two level logic styles, for functions where $P(V^C=1) \geq P(V^C=0)$, the complementary rather than the true output is likely to be implemented for reduced area. This again takes us back to the reverse case depicted in Figure 2(c) where the biased voters demonstrate significantly higher signal reliabilities.

To summarize, our analysis of biased and majority voting schemes has shown that as the ratio of faulty '1's to faulty '0's increases, biased voting configurations exhibit up to **66%** higher signal reliability.

III. FAULT PROBABILITY RATIO IN NASICS

In this section we address fault rates in the NASICs nanoscale fabric, and demonstrate the unequal fault probabilities for logic '1' and logic '0'. This paves the way for using biased voting schemes in this fabric to improve the yield.

A. Fabric overview and fault model

NASICs [9]-[14] is a computational fabric based on a 2D grid of semiconductor nanowires with external dynamic controls for data streaming and cascading. Cross-nanowire transistors (xnwFETs) are formed at selected cross-points to implement logic functions. In NASICs, the 2-stage dynamic NAND-NAND logic style is one of the logic families used [12]. A single NASIC circuit implementing a 2-stage logic function is called a NASIC *tile*. The output signals from the first stage NAND gates become the input signals for the transistors in the second stage NAND gate as shown in Figures 3(a) and 3(b). In Figure

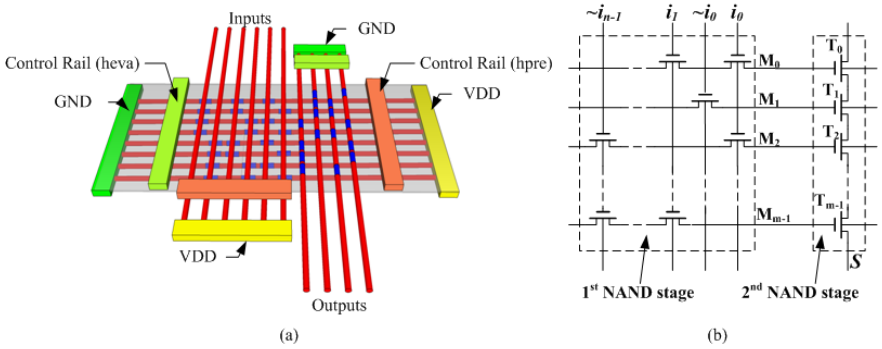


Figure 3. NASIC tiles: (a) A full adder implemented in NASICs (b) An n-input NASIC tile with the two NAND stages and the minterms shown.

3(b), input signals are denoted by i_j , where $\sim i_0$ is the complement for i_0. M_0 to M_{m-1} are the minterms generated by the first NAND stage and T_0 to T_{m-1} denote the transistors in the 2nd stage NAND gate. In each dynamic NAND gate in NASICs, the output is first pre-charged to '1' and evaluated through a series transistor stack as detailed in [12]. Since any transistor in the stack being switched off is enough to keep the output from evaluating to '0', faulty '0's are unlikely in high fan-in gates compared to faulty '1's. A single correctly turned off device will prevent wrong evaluation to a faulty '0'. In this section we prove this analytically.

In NASICs, high fan-in circuits are possible since delay/performance scales linearly with respect to fan-in as opposed to conventional CMOS where the trend is typically quadratic. This is due to the unique dynamic control schemes used, where successive cascaded stages are evaluated using different control signals. The series stack resistance of a given stage has limited impact during and after the pre-charge of the previous stage. This implies that during the evaluation of the current stage, only the linear impact of the capacitance affects the performance with increasing fan-in. This behavior has been verified through detailed simulations of device behavior and circuit characteristics. Additional details can be found in [23].

The types of defects that can occur in the NASICs fabric depend on the manufacturing pathway used. One possible manufacturing pathway has been detailed in [22]. Stuck-on transistors are the most prevalent in this pathway due to the ion implantation and metallization processes involved. Reliable manufacturing of nanowires up to a few microns in length has been demonstrated in [1],[2], so the frequency of broken nanowires is assumed to be negligible. Due to the prevalence of stuck-on defects, only this type of defects has been considered in our analysis and the probability of a transistor being stuck-on, denoted by P_d, represents the defect rate of the NASIC fabric. These defects are considered to occur independently of each other, since they are caused by local effects (e.g., lateral diffusion after ion implantation).

The notations that are used in this analysis are:

- n — Number of inputs for the logic function implemented
- m — Number of minterms generated by the first NAND stage
- S^C — Correct output of the logic function
- S^A — Actual output from a defective NASIC circuit implementing the logic function
- M_i^C — Correct i^{th} minterm expected from a defect-free circuit, $0 \le i \le m-1$
- M_i^A — Actual i^{th} minterm in a defective circuit
- T_i — Transistor gated by minterm M_i in the second NAND stage
- $P_{1/0} = P(S^A=1|S^C=0)$ — Probability of a faulty '1' at the output of a defective circuit (module)
- $P_{0/1} = P(S^A=0|S^C=1)$ — Probability of a faulty '0' at the output of a defective circuit (module)
- P_{Mf0} — $P(M_i^A=0|M_i^C=1)$; Probability of the minterm, M_i, being a faulty '0'

B. *Occurrence of a faulty '1'*

In a 2-stage NAND-NAND logic implementation, a '0' is produced at the output if all of the input signals (minterms) to the second stage NAND gate are '1's. Thus, in a NASIC tile, all of the xnwFETs in the second stage dynamic NAND gate must be correctly switched on to allow the output to evaluate to '0'. Hence, for a faulty '1' to be produced at the output, any one of the transistors has to be switched off to prevent evaluation to '0'. This will happen if any of the minterms carry an incorrect '0' and the transistor that the minterm is gating is not stuck-on (not defective). Thus the probability of a faulty '1' at the output can be written as,

$$P(S^A=1|S^C=0) = 1-P(S^A=0|S^C=0) = 1-P(\bigcap_{i=0}^{m-1} T_i^A = ON | T_i^C = ON) \quad (6)$$

$$P(T_i^A=ON|T_i^C=ON) = P(T_i=stuck\text{-}on \cup (T_i = not\ stuck\ on \cap M_i^A = 1|\, M_i^C = 1)) \quad (7)$$

Since $P_{Mf0} = P(M_i^A=0|M_i^C=1)$ and $P(T_i=stuck\text{-}on) = P_d$, we get,

$$P(T_i^A=ON|T_i^C=ON) = P_d+(1-P_d)(1-P_{Mf0}) \quad (8)$$

$$P(S^A=1|S^C=0) = 1-[P_d+(1-P_d)(1-P_{Mf0})]^m = 1-(1-P_{Mf0}+P_dP_{Mf0})^m \quad (9)$$

The above probability of a faulty '1' has been expressed in terms of the probability of a transistor being stuck-on, P_d, the number of minterms, m, and the probability of a minterm producing an incorrect '0', P_{Mf0}. The expression for P_{Mf0} is derived later.

C. *Occurrence of a faulty '0'*

When an input pattern that should produce a '1' at the output of a defect-free circuit arrives at such a 2-stage NAND-NAND circuit, all of the minterms carry logic '1' except for one minterm, M_x, that carries a logic '0'. Thus, only one transistor, say T_x, at the second stage NAND gate is correctly switched off in a defect-free circuit to keep the output at logic '1'. Hence, for a faulty '0' to occur in a defective circuit, transistor T_x should be incorrectly switched on while the other transistors remain correctly switched on, enabling evaluation to faulty '0'. Transistor T_x will incorrectly switch on if it is stuck-on or the minterm gating the transistor is incorrectly '1'. However, we assume that the input signals to the two-stage NAND-NAND circuit are error-free. Also, since we are considering stuck-on type of defects in this model, the minterms can never carry incorrect '1's. As a result, the only way transistor, T_x, can be incorrectly switched on is if it is defective (stuck-on); Thus, $P(T_x^A = ON|T_x^C = OFF) = P_d$. The expression for the probability of a faulty '0' is,

$$P(S^A=0|S^C=1) = P(\{\bigcap_{i=0;i\neq x}^{m-1} T_i^A = ON|T_i^C = ON\} \cap \{T_x^A = ON|T_x^C = OFF\}) \quad (10)$$

Substituting (8) into (10), we get,

$$P(S^A=0|S^C=1) = P_d(1-P_{Mf0}+P_dP_{Mf0})^{m-1} \quad (11)$$

In this model, the probability of a minterm being a faulty '0', P_{Mf0}, is entirely dependent on the transistors of the first stage NAND gates being defective. In the development of the expression for P_{Mf0}, we make a simplifying assumption that logic functions are implemented in a 2-level Sum of Products form without logic minimization. Hence, for a logic function with n inputs, every NAND gate in the first stage has n transistors. Each of the first stage NAND gates should output a '0' for one particular input pattern and output a '1' for all of the rest. For each of these input patterns that should produce an output '1', one or more transistors will be correctly switched off to keep the output at '1'. Thus, for a minterm to be a faulty '0', one or more transistors needs to be stuck-on depending on the input pattern. For instance, in a 3-input logic function implemented in the NASIC fabric, at any one of the first stage NAND gates, there are 7 input patterns that should produce an output of '1' at that NAND gate. 1 out of those 7 input patterns will require all 3 transistors in the gate to be stuck-on to produce a faulty '0'. Three of the input patterns will require 2 transistors to be stuck-on and the remaining 3 input patterns will require only one

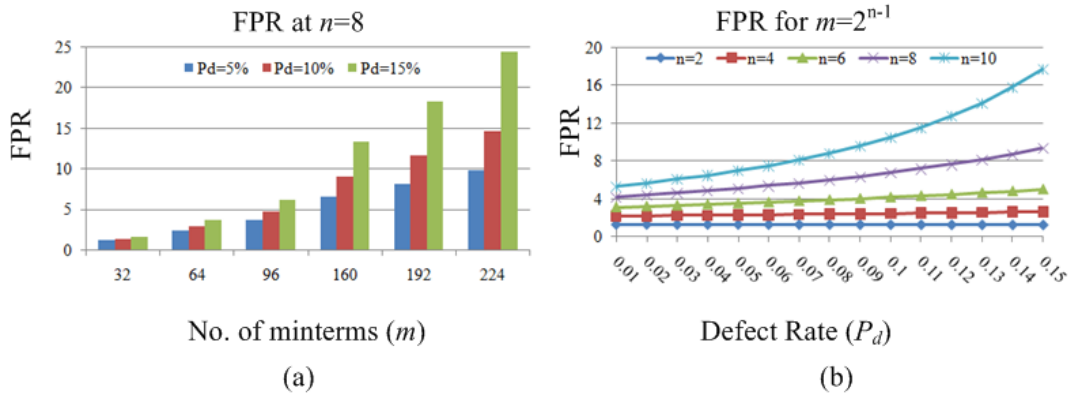


Figure 4. Fault Probability Ratio as a function of (a) number of minterms for n=8 at defect rates of 5%, 10% and 15%, (b) defect rate for a range of fan-in (n) when $m=2^{n-1}$

transistor to be stuck-on to produce a faulty '0'. Assuming all input patterns are equally probable, P_{Mf0} for this 3-input logic function would be,

$$P_{Mf0} = \frac{1}{7}(P_d^3 + 3P_d^2 + 3P_d) \tag{12}$$

Using the binomial expansion, an expression for P_{Mf0} for an n-input logic function can be obtained:

$$P_{Mf0} = \frac{1}{2^n - 1}[(1+P_d)^n - 1] \tag{13}$$

By substituting (13) in (9) and (11), probabilities of faulty '1's and faulty '0's at the output of a NASIC tile with no structural redundancy can be found. Thus, the FPR is a function of the fault probability P_d, the number of inputs of the logic function n, and the number of minterms m.

Figure 4(a) shows the FPR of a NASIC tile with a fan-in of n=8 for an increasing number of minterms (m) at three different defect rates. It is observed that the FPR rises with increasing number of minterms. This is expected since an increase in the number of transistors in the 2nd stage NAND gate makes faulty '0's less likely and faulty '1's more likely. Furthermore, for a certain NASIC tile, the FPR is greater for a higher value of the defect rate, P_d. For instance, the FPR is 8.1 for a tile with n=8 and m=160 at a defect rate of 5%, and 18.22 for a defect rate of 15%, suggesting that the reliability improvement is greater if biased voters are used when the defect rates are higher. This can be better observed from Figure 4(b) that shows the FPR for a range of defect rates up to 15%. Defect rates of up to 15% are considered because any density advantage over CMOS is lost beyond this rate [11]. In these plots, the average case (i.e., a symmetric function) was considered where the logic function implemented should produce (in the defect-free case) a '1' output for half of the 2^n input patterns and '0' for the remaining half so $m=2^{n-1}$.

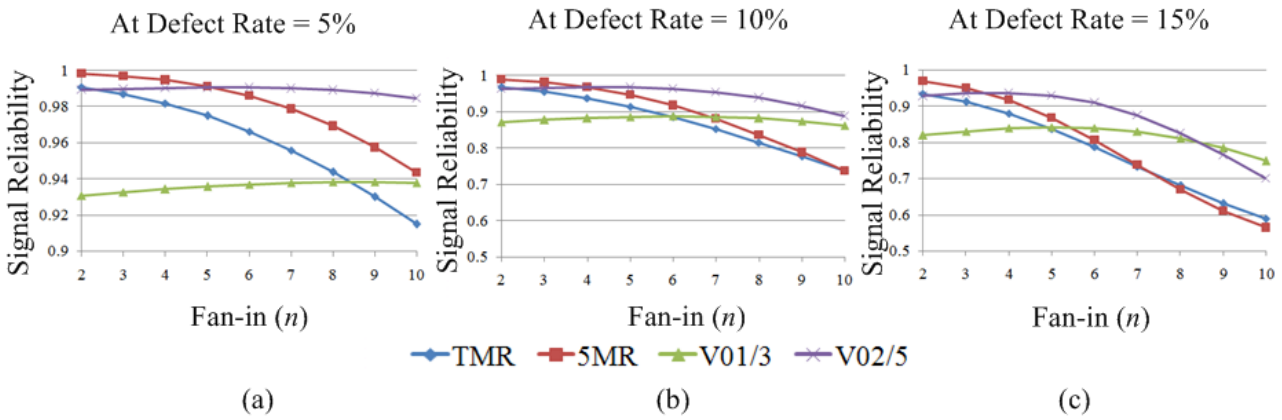
Figure 4(b) shows that although the FPR rises with the defect rate, the rate of increase is more marked for circuits with higher fan-in (n). Moreover, for a particular defect rate, the FPR is greater for circuits with higher fan-in. For instance, at a defect rate of 12%, a tile with a fan-in of 6 had an FPR of 4.5 whereas a tile with a fan-in of 10 had an FPR of 12.7. This implies that using biased voters will provide increased yield for circuits with a high number of inputs (fan-in) and minterms at the high defect rates that are characteristic of nanoscale fabrics.

IV. Biased Voters in NASICs

In this section, the probability expressions for faulty '1's and faulty '0's derived in Section 3, are used to compare the signal reliabilities for circuits implemented with biased and majority voting schemes. Figure 5 shows the reliabilities for n-input NASIC circuits for the voting schemes introduced in Section 2.

As we have previously observed for a given defect rate, there is a minimum fan-in (n) before biased voting schemes show a higher reliability over majority voting schemes. Moreover, this required minimum value of fan-in decreases with increasing defect rates. For example, at a defect rate of 5%, the $V_0^{1/3}$ biased voting scheme has a greater reliability than the TMR scheme only for NASIC circuits with n=9 or greater. However, at a defect rate of 15%, the $V_0^{1/3}$ scheme has a higher reliability even for circuits that have a fan-in of 6. This suggests that at the high defect rates that nanoscale fabrics are subject to, using biased voting schemes will provide a greater reliability even for circuits with low fan-in.

For a particular defect rate, the biased voting schemes give a higher reliability as the circuit fan-in increases due to the increasing FPR discussed in the previous section. For instance, the $V_0^{1/3}$ biased scheme has a 27% greater reliability compared to the TMR scheme while the $V_0^{2/5}$ biased scheme has 24% higher reliability than the 5MR scheme. The reliability advantage



will be even greater when $P(V^C=0) \neq P(V^C=1)$ as shown in Section 2. This implies that biased voters could be employed at key architectural points in the design, specifically at the outputs of high fan-in stages, for greater yield, while carefully managing yield-area tradeoffs.

The biased voting schemes may also be more area efficient than majority voters or, at the worst case, consume the same area when implemented with 2-level logic such as used in the NASIC fabric. This is because the number of minterms for a biased voter will be less than or equal to the number of minterms for a majority voter with the same number of inputs. This implies that the effective yield (i.e., yield divided by the area increase factor) for biased voting schemes may be higher.

V. CONCLUSIONS

In this paper, we have analyzed the increase in signal reliability gained by using biased voters in cases where there is an imbalance between the probabilities of faulty '0's and '1's. We have shown that beyond a certain Fault Probability Ratio, biased voting schemes exhibit a higher reliability than majority voting schemes. We have taken the NASIC fabric as a specific case and have shown that faulty '1's can be as much as 12 times more likely than faulty '0's for a circuit with a fan-in of 10. Consequently, biased voting schemes were shown to have almost 27% higher signal reliability compared to majority voting schemes for these circuits. Overall, biased voters showed increased reliability with greater Fault Probability Ratios. These biased voters are applicable to other fabrics where unequal fault rates exist.

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